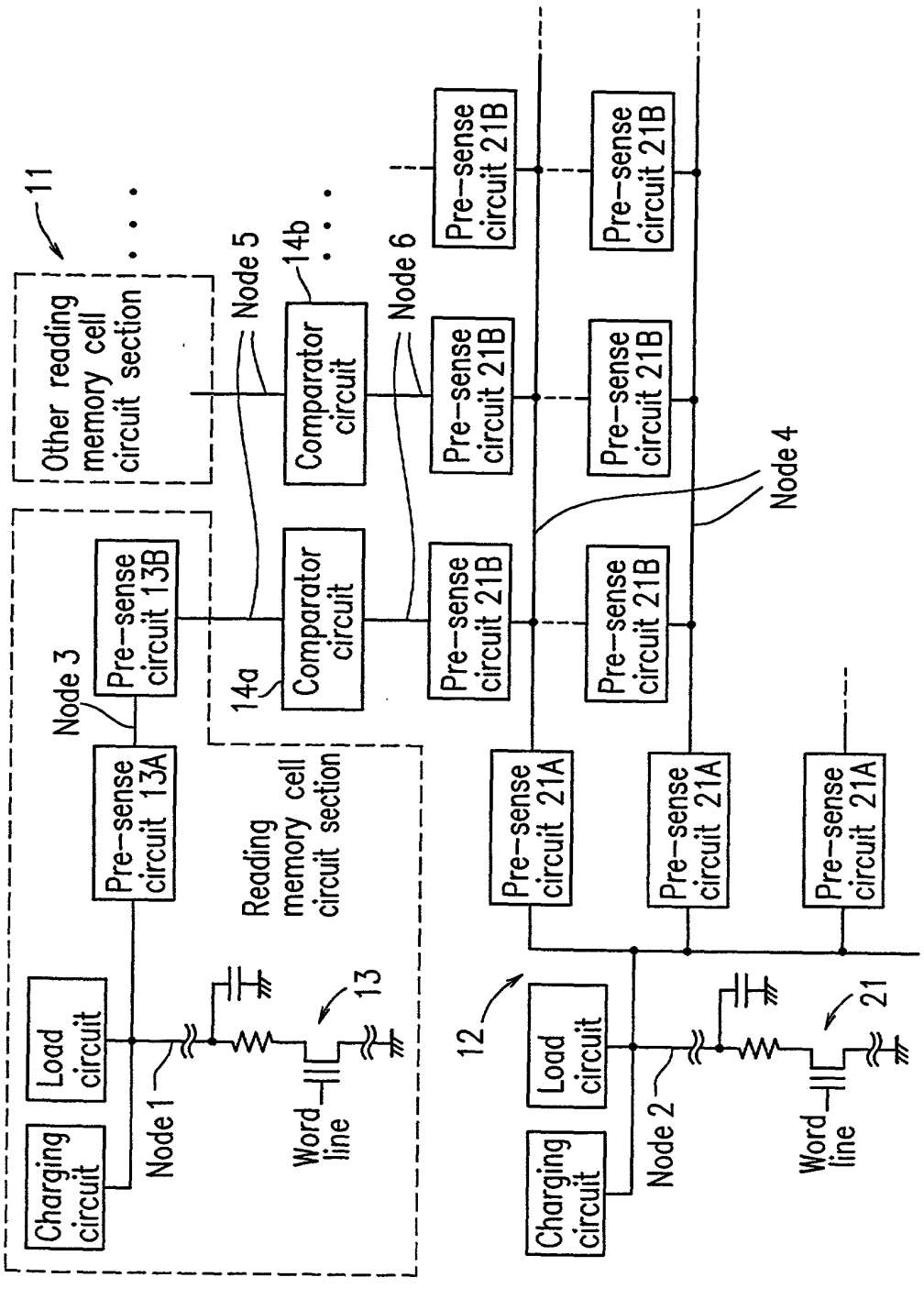


FIG. 1

FIG. 2

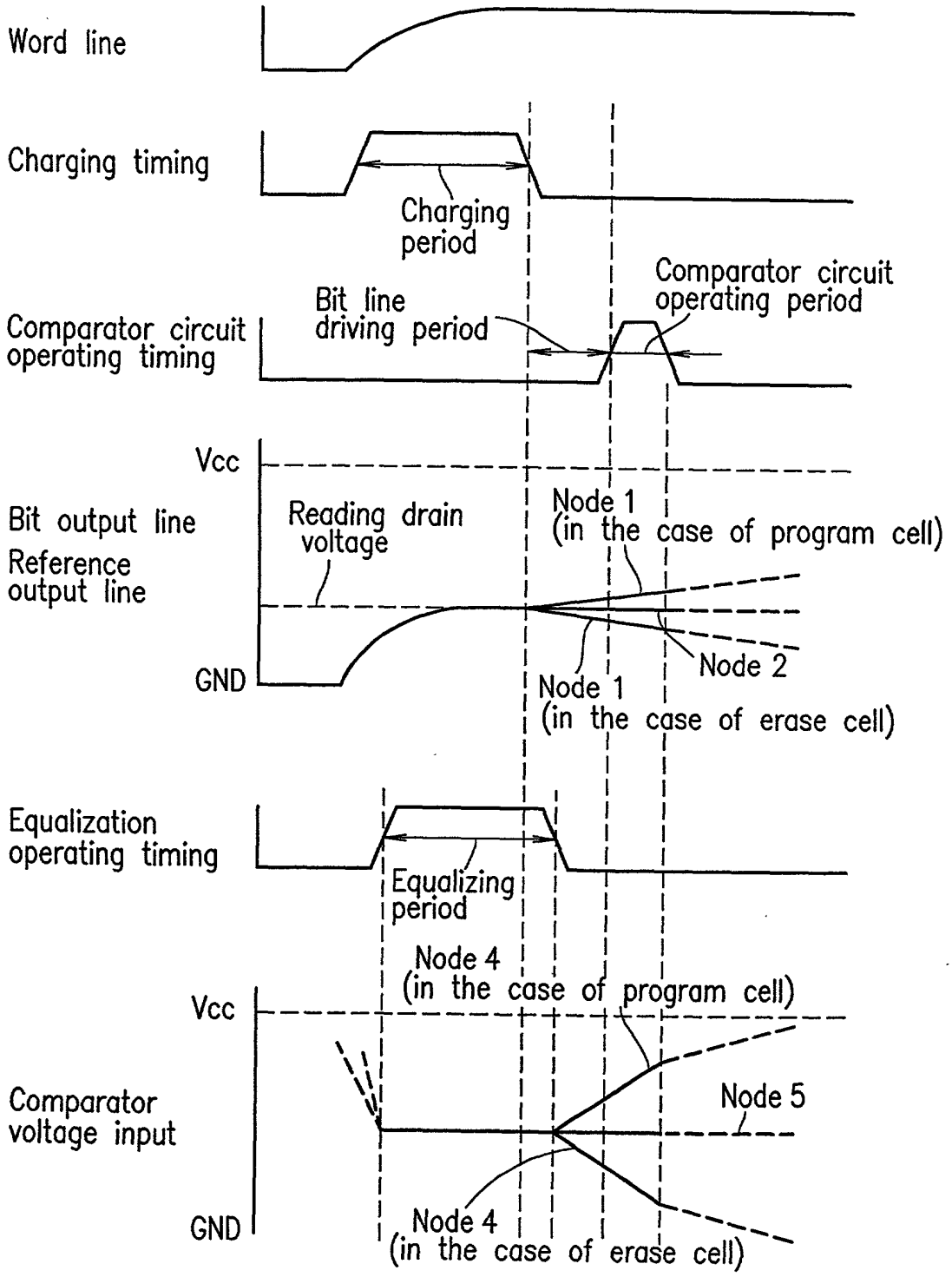

Word line
Charging timing
Charging period
Comparator circuit operating timing
Bit line driving period
Comparator circuit operating period
Vcc
Bit output line
Reading drain voltage
Node 1 (in the case of program cell)
Reference output line
GND
Node 2
Node 1 (in the case of erase cell)
Equalization operating timing
Equalizing period
Node 4 (in the case of program cell)
Vcc
Comparator voltage input
Node 5
GND
Node 4 (in the case of erase cell)

FIG. 3

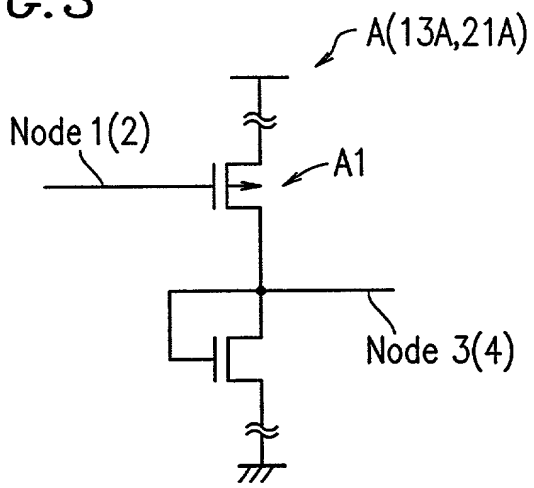

A(13A,21A)
Node 1(2)
A1
Node 3(4)

FIG. 4

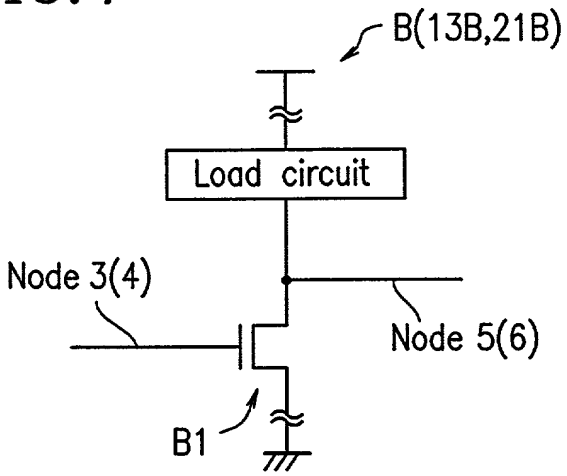

B(13B,21B)
Load circuit
Node 3(4)
Node 5(6)
B1

FIG.5

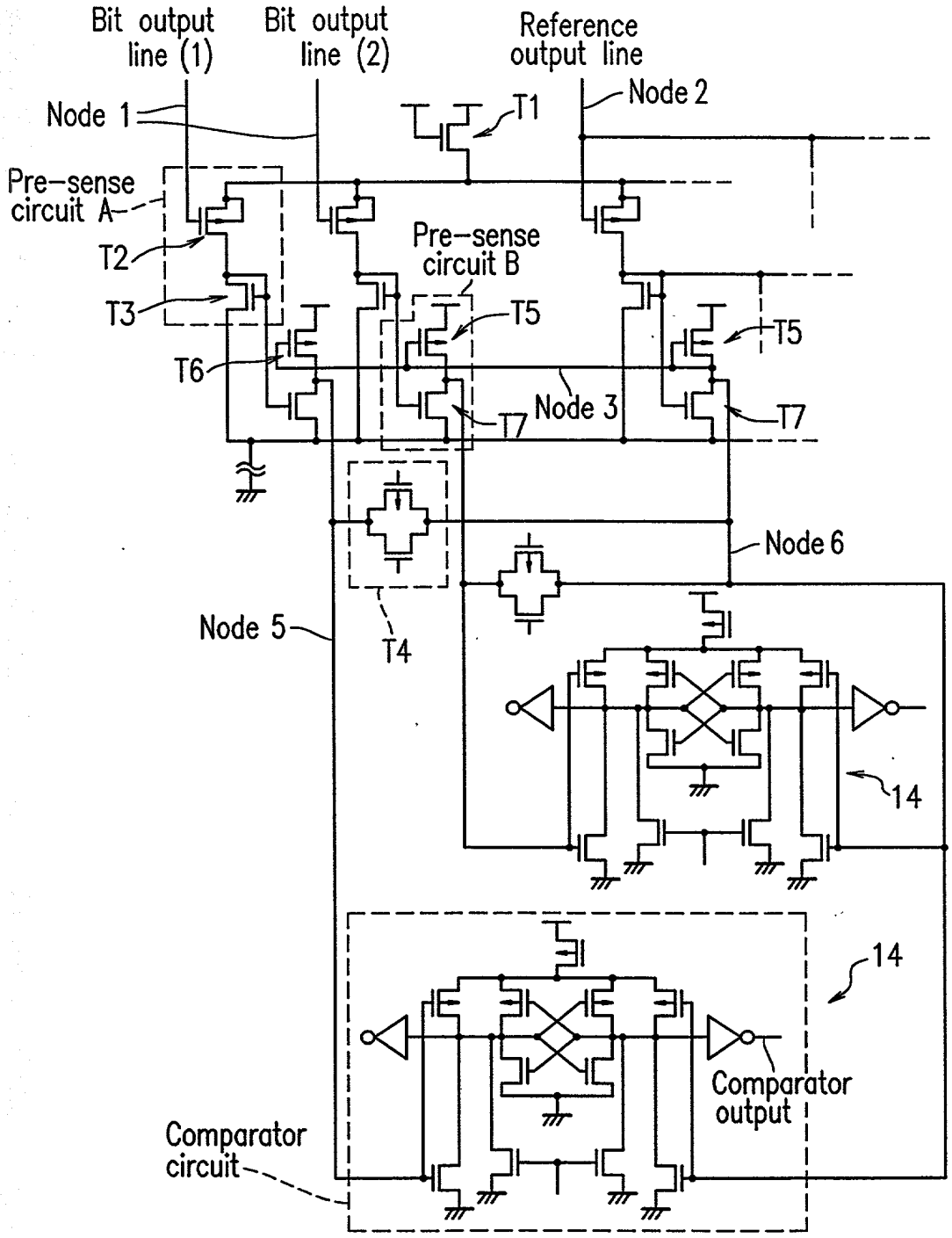

Bit output line (1)
Bit output line (2)
Reference output line
Node 1
Node 2
T1
Pre-sense circuit A
T2
T3
Pre-sense circuit B
T5
T5
T6
Node 3
T7
T7
Node 6
Node 5
T4
14
14
Comparator output
Comparator circuit

FIG. 6

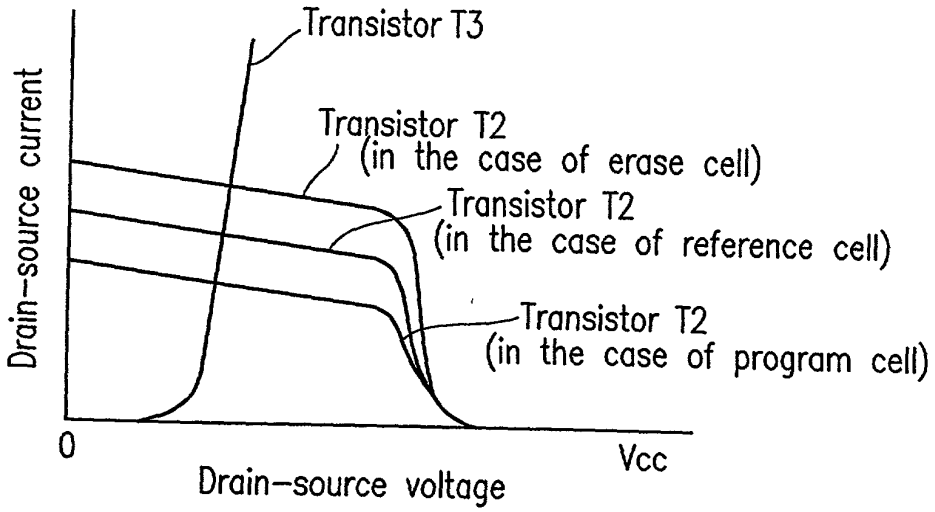

Transistor T3
Transistor T2
(in the case of erase cell)
Transistor T2
(in the case of reference cell)
Transistor T2
(in the case of program cell)
Drain-source current
0
Vcc
Drain-source voltage

FIG. 7

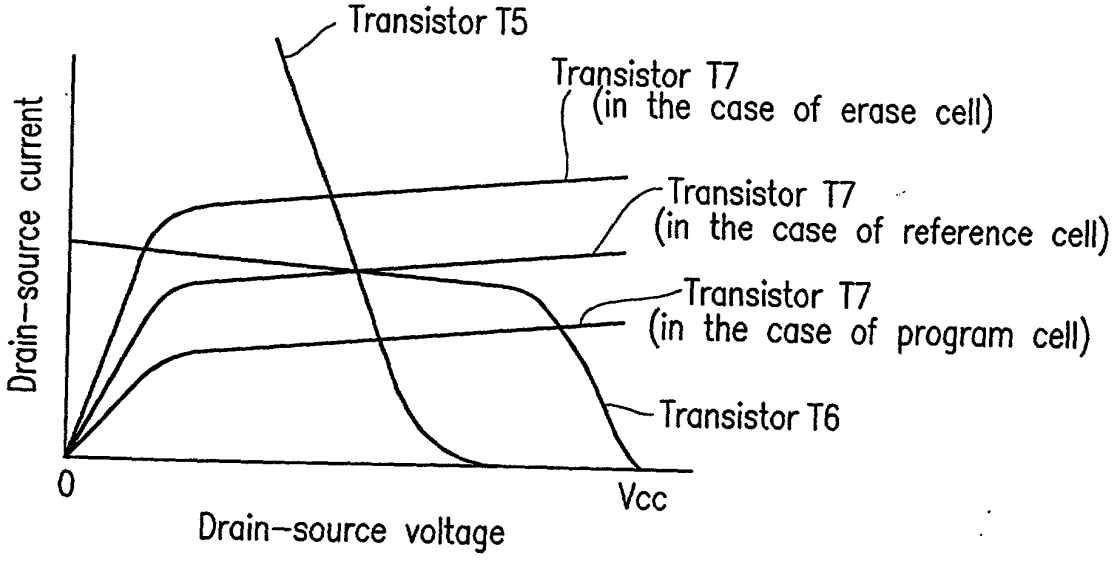

Transistor T5
Transistor T7
(in the case of erase cell)
Transistor T7
(in the case of reference cell)
Transistor T7
(in the case of program cell)
Transistor T6
Drain-source current
0
Vcc
Drain-source voltage

FIG. 8

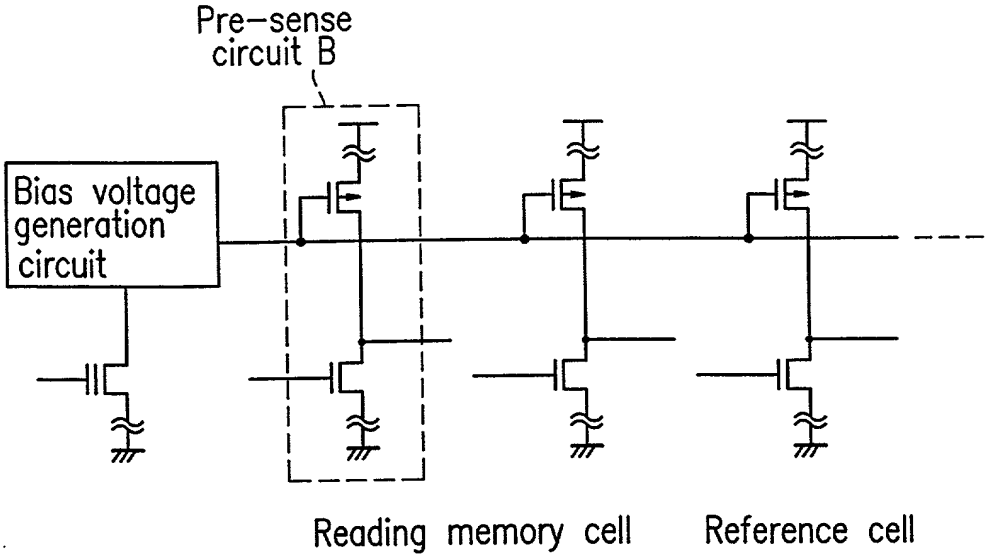

Pre-sense circuit B
Bias voltage generation circuit
Reading memory cell
Reference cell

FIG. 9

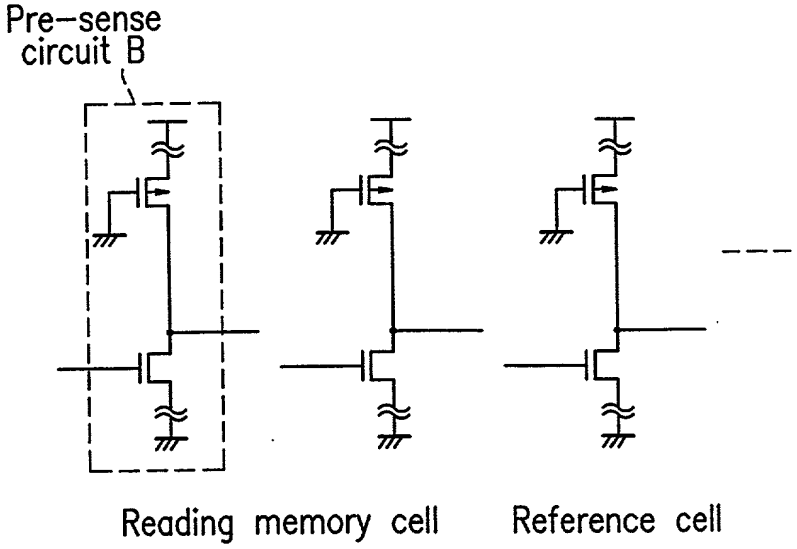

Pre-sense circuit B
Reading memory cell
Reference cell

FIG. 10

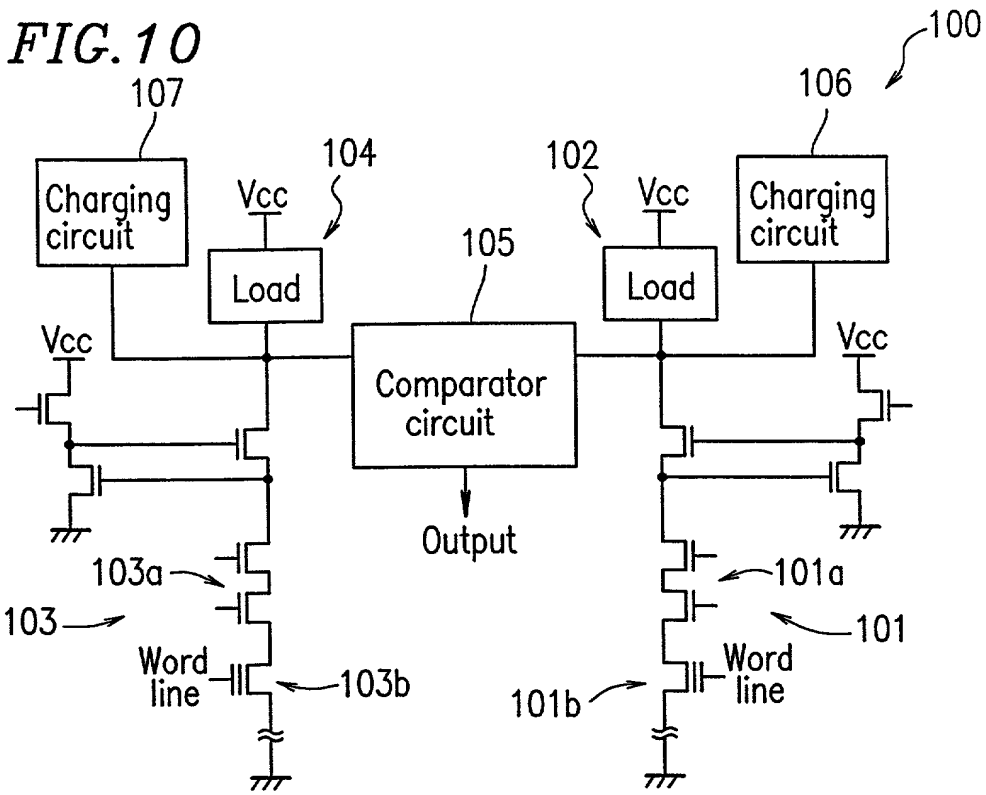

100
106
107
Charging circuit
104
Vcc
Load
102
Vcc
Load
Charging circuit
105
Vcc
Comparator circuit
Vcc
Output
103a
101a
103
101
Word line
103b
101b
Word line

FIG. 11

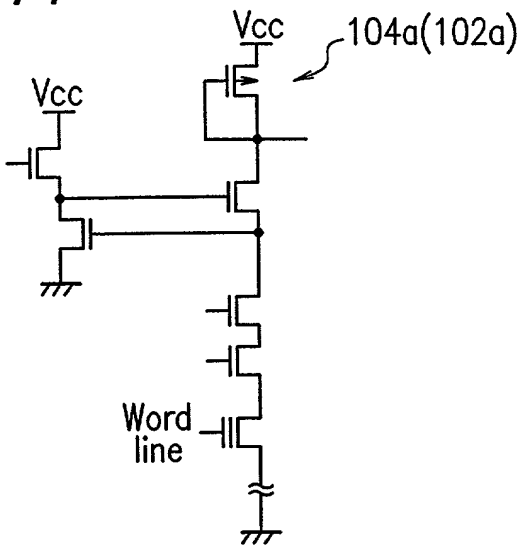
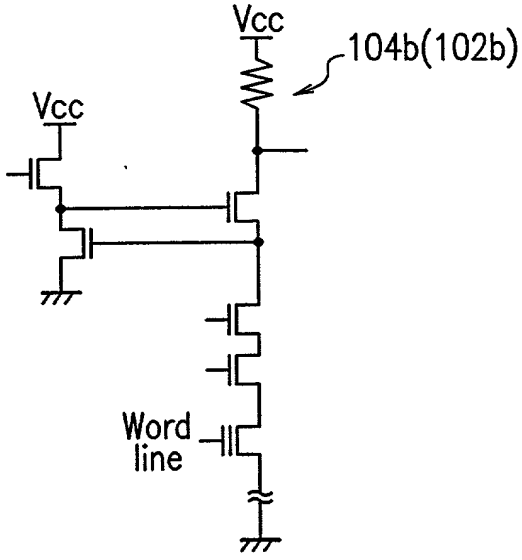


FIG. 12



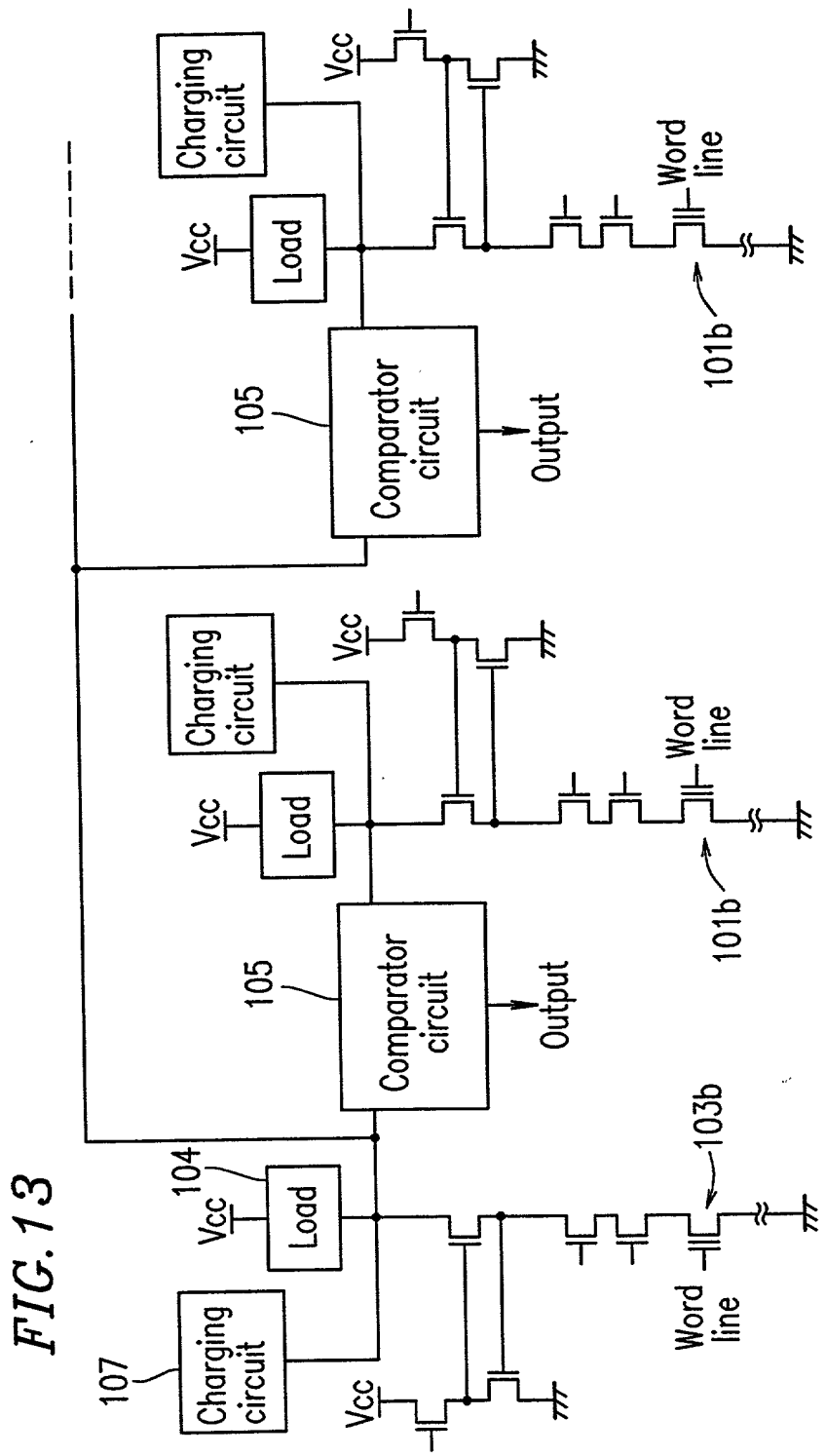

Charging circuit
Vcc
Load
Word line
101b
105
Comparator circuit
Output
104
103b
107

FIG. 13

FIG. 14

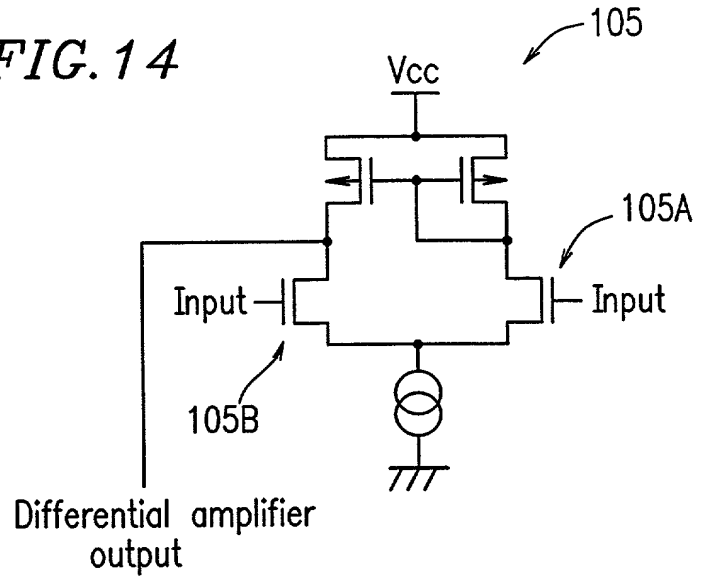
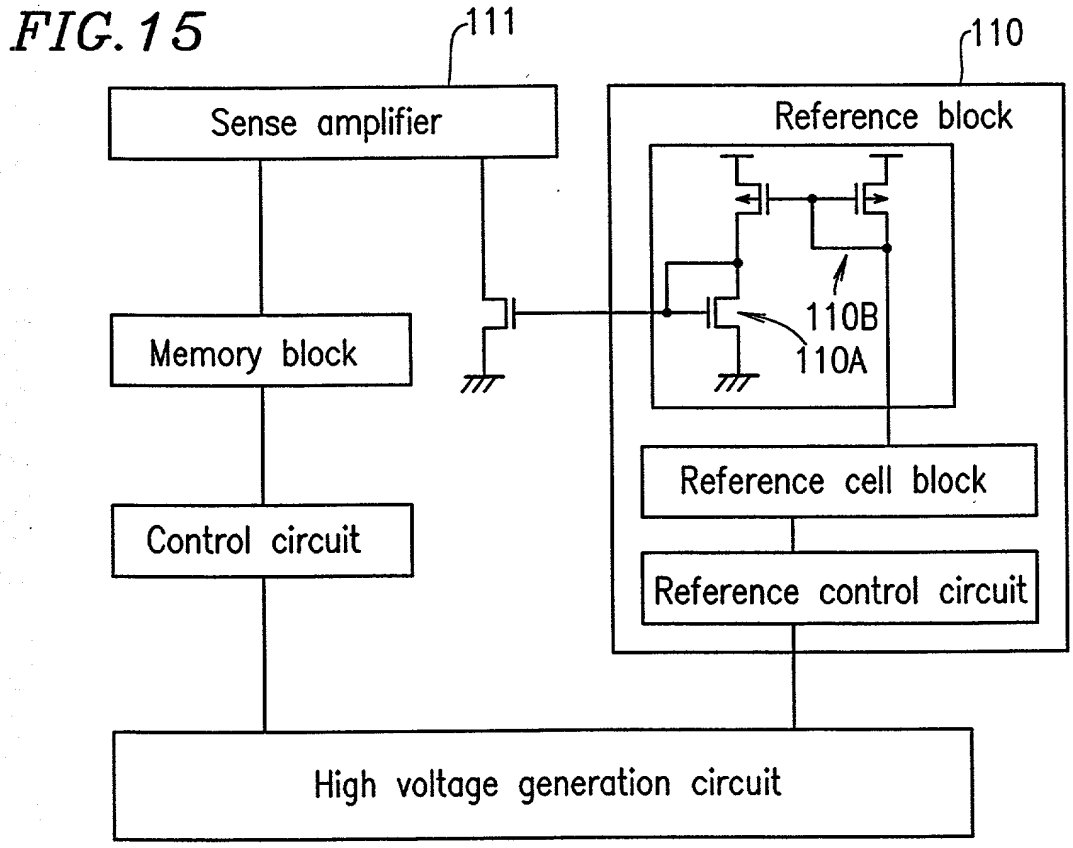

105
Vcc
105A
Input
Input
105B
Differential amplifier output

FIG. 15


111
110
Sense amplifier
Reference block
110B
110A
Memory block
Reference cell block
Control circuit
Reference control circuit
High voltage generation circuit

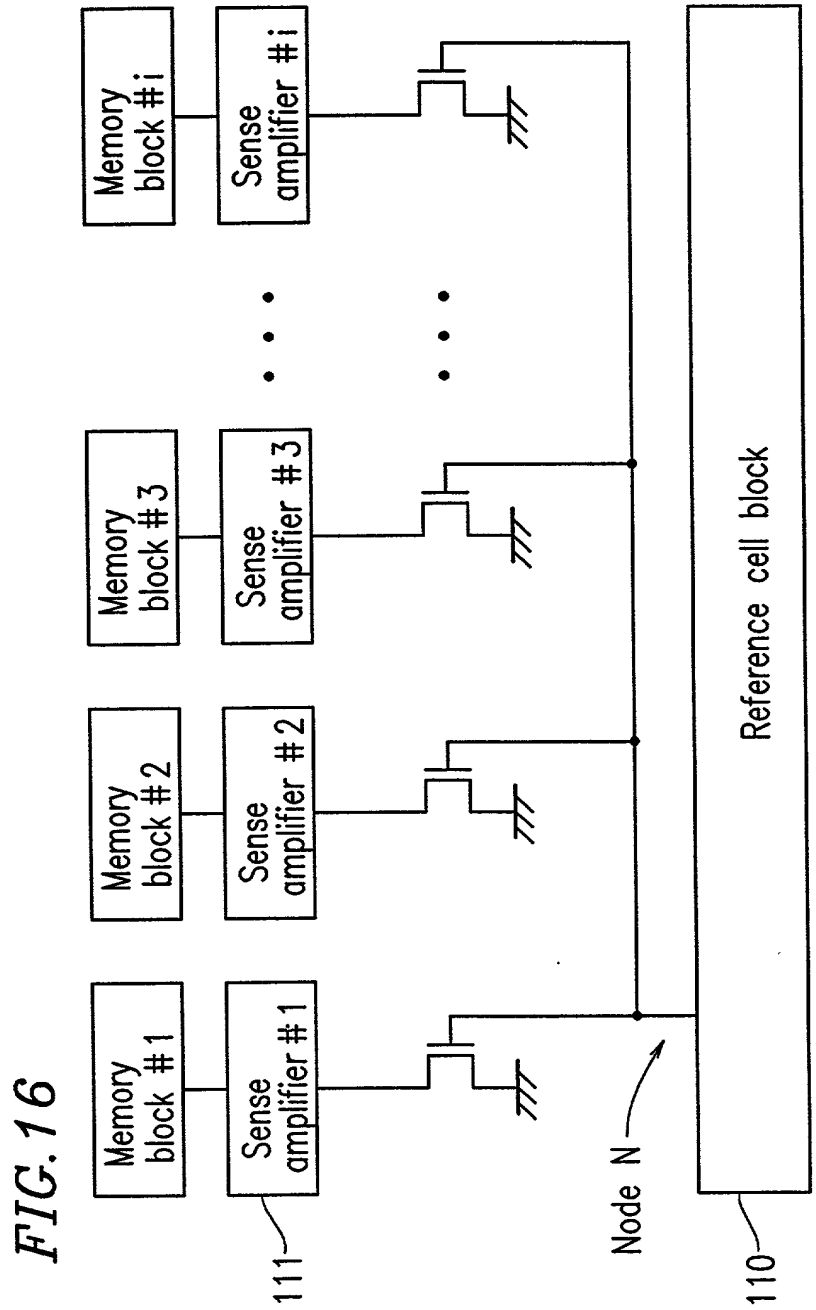
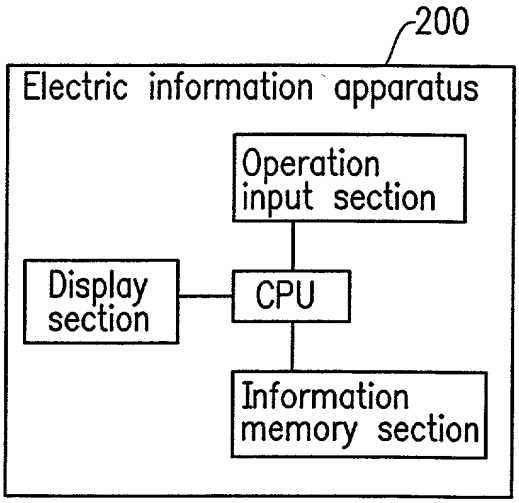

Memory block #1
Sense amplifier #1
Memory block #2
Sense amplifier #2
Memory block #3
Sense amplifier #3
Memory block #i
Sense amplifier #i
Reference cell block
Node N
111
110

FIG. 16

FIG. 17


200
Electric information apparatus
Operation input section
Display section
CPU
Information memory section

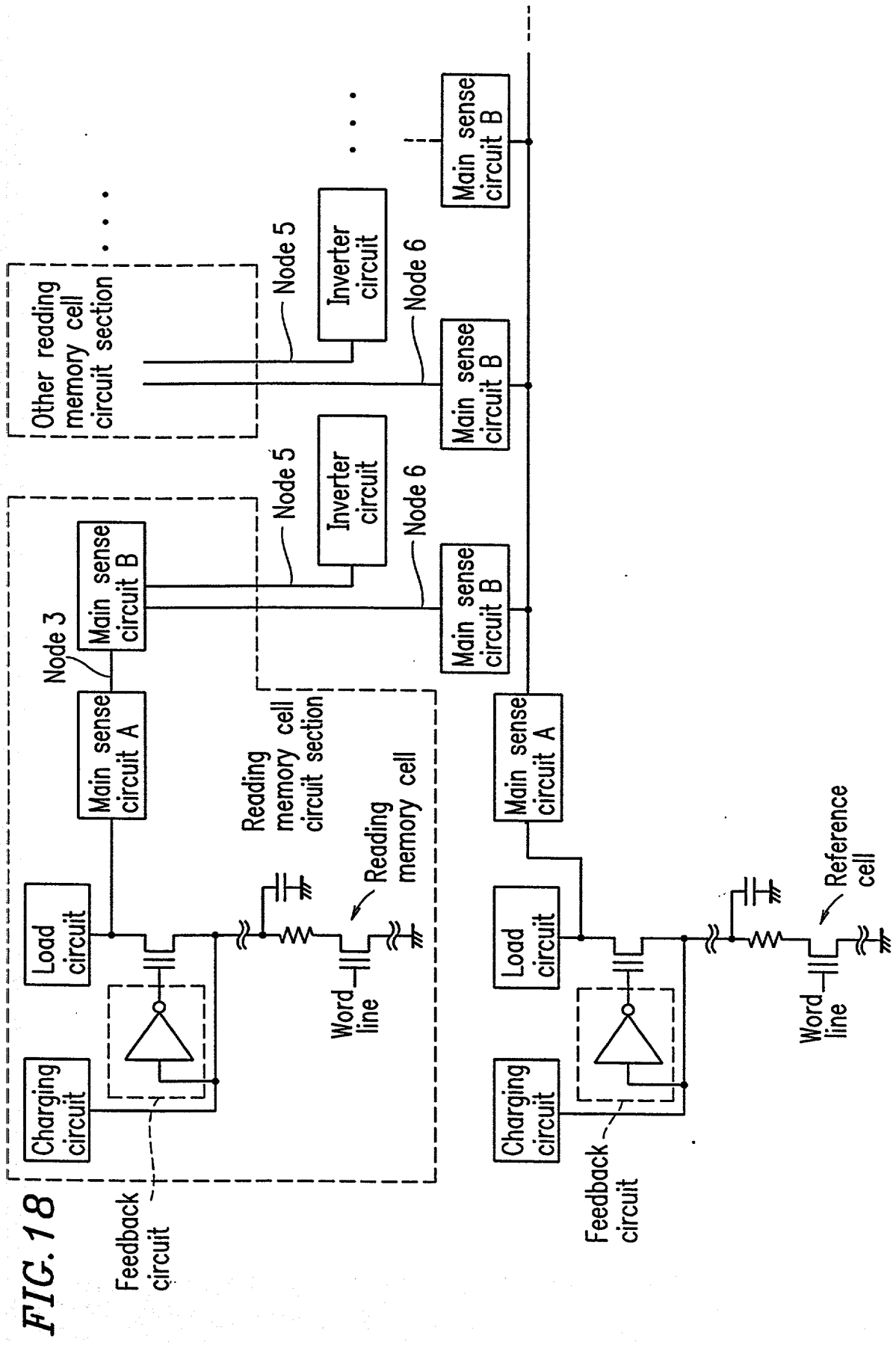
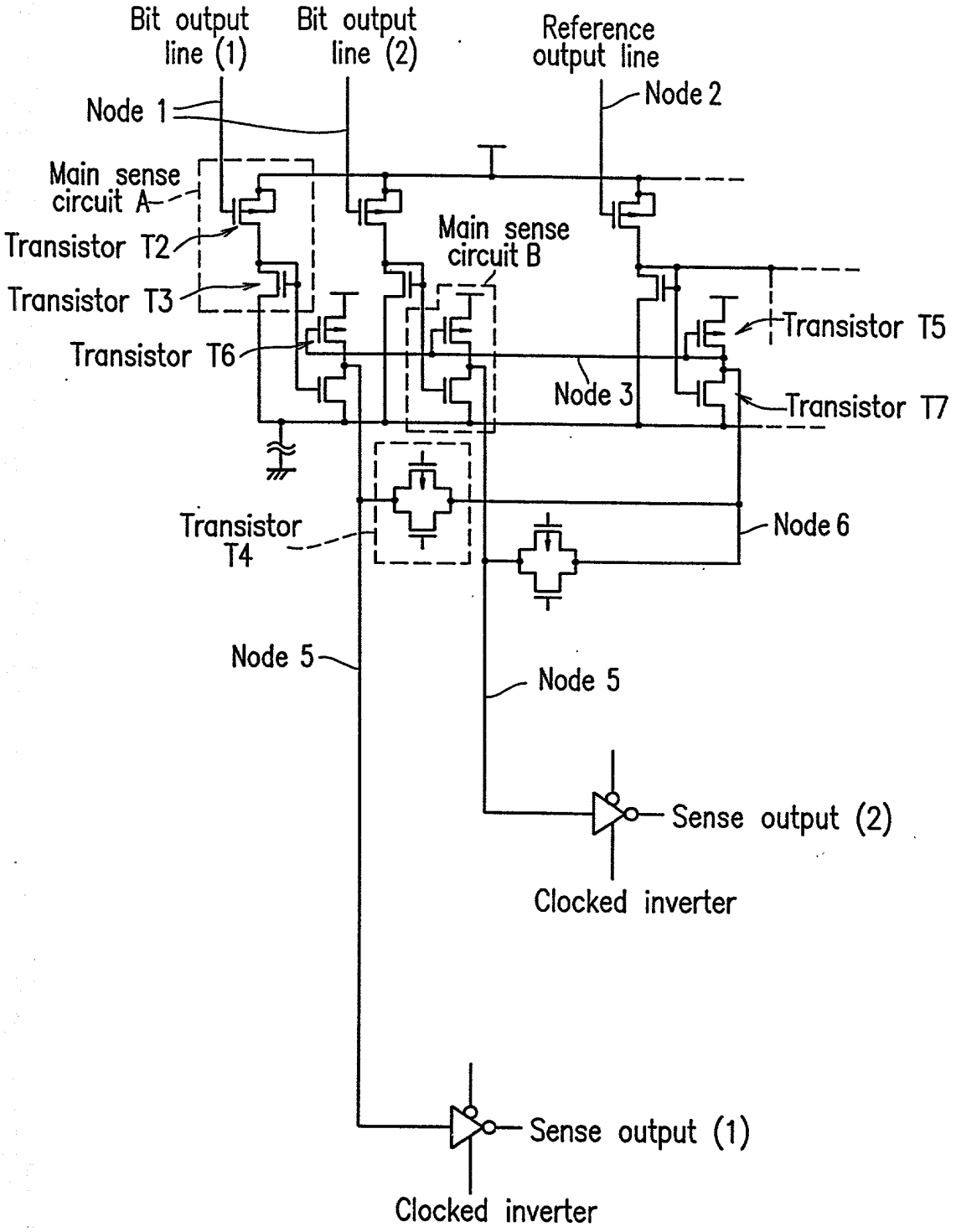

Other reading memory cell circuit section
Node 5
Inverter circuit
Node 6
Main sense circuit B
Main sense circuit B
Main sense circuit B
Main sense circuit B
Node 3
Main sense circuit A
Main sense circuit A
Reading memory cell circuit section
Reading memory cell
Reference cell
Load circuit
Load circuit
Charging circuit
Charging circuit
Word line
Word line
Feedback circuit
Feedback circuit

FIG. 18

FIG. 19


Bit output line (1)
Bit output line (2)
Reference output line
Node 1
Node 2
Main sense circuit A
Transistor T2
Transistor T3
Transistor T6
Main sense circuit B
Transistor T5
Node 3
Transistor T7
Transistor T4
Node 6
Node 5
Node 5
Sense output (2)
Clocked inverter
Sense output (1)
Clocked inverter